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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/027,639	12/19/2001	Sung-Muk Lim	9903-44	1485

7590 05/06/2005

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EXAMINER	
TRAIL, ALLYSON NEEL	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,639	LIM ET AL.	
	Examiner	Art Unit	
	Allyson N. Trail	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9-21 and 23-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-21 and 23-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/19/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Receipt is acknowledged of the amendment filed February 17, 2005.

Remarks

2. The current amendment has amended claims 1, 9, 15, 18, and 25. Claims 2, 8, and 22 have been cancelled.

Claim Objections

3. Claim 18 is objected to because of the following informalities:

Re claim 18, lines 12 and 13: replace "product" with --products--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-7, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in view of Shyu et al (5,923,792).

Iwakiri et al teaches the following in regards to claims 1, 7, and 25:

Figure 1 shows the following:

A reference character set is inputted via the keyboard 2a. The reference character set is then shown on the screen 2b and the character set information is sent to the information processing device 1. As seen on the screen 2b, the character set

may include a barcode or letters. The semiconductor wafer 10 is placed on a turntable 4. The laser head 21, which is connected to the engraving device 2, engraves the markings onto the wafer 10. The turntable spins to allow the reading camera 31, to read the engraved markings off of the wafer. The image read with the reading device appears on the display screen 3a and is also sent to the information processing device for comparison. In this method the features of the markings are extracted and the features produce character data (as seen on the screen 3a).

Iwakiri et al teaches the following in regards to claims 2 and 26:

Figure 2 shows a block diagram disclosing steps of determining if the marking is defective and classifying it as so. The steps include comparing the character data to the reference character set.

Iwakiri et al teaches the following in regards to claims 3 and 4:

As discussed above, the character set is inputted directly using a keyboard.

Iwakiri et al teaches the following in regards to claims 5 and 6:

"Engraving information for engraving the identification mark is inputted into the engraving device body 2 via a keyboard 2a, a computer mouse (not shown) or the like." (Col. 3, lines 1-3). As shown in figure 1, the engraving information is shown as barcode.

Iwakiri et al's teachings above fail to teach a using an optical character recognition technique and comparing the actual character makings to a selected group of predefined characters and if one of the characters is not recognized, determining the actual character markings to be defective.

Shyu et al teaches the following in regards to claims 1 and 25:

Figure 2 illustrates a process of accepting or rejecting a document to be scanned and optically recognized. As shown in the figure the document is manual a comparison process is conducted, where actual characters are compared with predefined characters. As seen in the flow chart, if the form does not pass "form recognition" the document is rejected.

In view of Shyu et al's teachings it would have been obvious to one of ordinary skill in the art at the time the invention was made to use an optical character recognition unit to recognize the character image on the semiconductor taught by Iwakiri et al. Iwakiri et al teaches taking an image of the characters and displaying the image on a screen for comparison to a reference character set. One would be motivated to use an OCR technique if the characters were not imaged clearly. OCR techniques perform comparisons in order to best suggest what the character actually is. If the actual character is not recognized by the OCR technique it would be beneficial to determine so, in order to mark the semiconductor as defective as taught by Shyu et al. This would reduce wasted time in attempting to read the characters on the semiconductor.

6. Claims 9-14 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in combination with Shyu et al (5,932,792) and in further view of Akamatsu (5,768,290).

Iwakiri et al's teachings in combination with Shyu et al's teachings are discussed above. The combination however fails to teach testing external terminals of the semiconductor products.

Akamatsu teaches the following in regards to claims 9 and 27:

"When testing at the wafer level is completed and the step for carrying out a fuse program to determine a pass/failure is completed, the semiconductor integrated circuit devices on the wafer are separated into chips in a dicing step. The semiconductor integrated circuit device formed as a chip is packaged (molded) in a mold step S3. Following completion of mold step S3, final testing for each individual semiconductor integrated circuit device is carried out (step S4). In this final test step S4, a signal is input/output via an external pin terminal for each semiconductor integrated circuit device to carry out a function test similar to that carried out at the wafer level with respect to each input/output terminal (a pin terminal is electrically connected to respective internal signal input/output pads: when non-defective)." (Col. 2, lines 19-32).

The limitations of claims 10-14 are taught above by Iwakiri et al.

In view of Akamatsu's teachings it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Akamatsu with the combination of the teachings by Iwakiri et al and Shyu et al. The combination of Iwakiri et al and Shyu et al's teachings teach a method of detecting defective markings on a semiconductor wafer. The purpose is to classify defective semiconductors in order to avoid dispensing the defective semiconductors to the public. Akamatsu teaches testing the actual semiconductor wafer and not the identifying marking that is on the wafer. One would be motivated to also test the actual semiconductor before dispensing the semiconductor to the public along with testing the identifying marking which is present on the surface of the wafer. It is clear that the teachings of both Iwakiri et al and Shyu et al are aimed at dispensing a working and

functioning semiconductor and therefore testing the actual semiconductor would be an obvious step before dispensing the product.

7. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in combination with Shyu et al (5,943,551) and in further view of Caldwell et al (5,575,136).

Iwakiri et al's teachings in combination with Shyu et al's teachings are discussed above. The combination however fails to teach transferring the semiconductor product onto a carrier tape.

The limitations of claims 16 and 17 are taught above by Iwakiri et al.

Caldwell et al teaches the following in regards to claim 15:

Figure 2 shows the semiconductor device being placed on the carrier tape 10.

In view of Caldwell et al's teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Calwell et al with the combination of the teachings by Iwakiri et al and Shyu et al. The combination of Iwakiri et al and Shyu et al's teachings teach a method of detecting defective markings on a semiconductor wafer during the manufacturing process. Caldwell et al teaches transferring the semiconductor product onto a carrier tape. One would be motivated to perform the transferring step simply because placing the product onto carrier tape is a part of a typical manufacturing process. Carrier tapes are generally used to protect and hold the semiconductor device in place while making any additional cuts, etching or placing the semiconductor onto a circuit board.

8. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in combination with Shyu et al (5,943,551) and in further view of Stubblefield et al (6,043,101).

Iwakiri et al's teaches in combination with the teachings of Shyu et al are discussed above. These teachings include limitations disclosed in claims 19-21. The combination however fails to teach an unloading unit for separating passing or failing products.

Stubblefield et al teaches the following in regards to claim 18:

Claim 20, which discloses, "the method according to claim 19 wherein said step of discarding comprises the steps of separating said chips from said wafer and sorting said failed chips into a bin separate from said chips that passed said series of tests."

In view of Stubblefield et al's teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a unloading unit as taught by Stubblefield et al. The teachings of Iwakiri et al in combination with Shyu et al disclose separating readable characters on semiconductor and unrecognizable characters on semiconductors. One would be motivated to include an unloading unit in order to clearly separate the correct or acceptable semiconductors from the defective semiconductors.

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in combination with Shyu et al (5,943,551) and Stubblefield et al (6,043,101) and in further view of Akamatsu (5,768,290).

Iwakiri et al's teachings in combination with Shyu et al's and Stubblefield et al teachings are discussed above. The combination however fails to teach testing external terminals of the semiconductor products.

Akamatsu's teachings are discussed above.

In view of Akamatsu's teachings it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Akamatsu with the combination of the teachings by Iwakiri et al and Shyu et al. The combination of Iwakiri et al and Shyu et al's teachings teach a method of detecting defective markings on a semiconductor wafer. The purpose is to classify defective semiconductors in order to avoid dispensing the defective semiconductors to the public. Akamatsu teaches testing the actual semiconductor wafer and not the identifying marking that is on the wafer. One would be motivated to also test the actual semiconductor before dispensing the semiconductor to the public along with testing the identifying marking which is present on the surface of the wafer. It is clear that the teachings of both Iwakiri et al and Shyu et al are aimed at dispensing a working and functioning semiconductor and therefore testing the actual semiconductor would be an obvious step before dispensing the product.

10. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwakiri et al (6,377,866) in combination with Shyu et al (5,943,551) and Stubblefield et al (6,043,101) and in further view of Caldwell et al (5,575,136).

Iwakiri et al's teachings in combination with Shyu et al's and Stubblefield et al teachings are discussed above. The combination however fails to teach transferring the semiconductor product onto a carrier tape.

See Caldwell et al's teachings above.

In view of Caldwell et al's teaching it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Calwell et al with the combination of the teachings by Iwakiri et al, Shyu et al, and Stubblefield et al. The combination of Iwakiri et al and Shyu et al's teachings teach a method of detecting defective markings on a semiconductor wafer during the manufacturing process. Caldwell et al teaches transferring the semiconductor product onto a carrier tape. One would be motivated to perform the transferring step simply because placing the product onto carrier tape is a part of a typical manufacturing process. Carrier tapes are generally used to protect and hold the semiconductor device in place while making any additional cuts, etching or placing the semiconductor onto a circuit board.

Response to Arguments

11. Applicant's arguments filed February 17, 2005 with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection. The current amendment added specific limitations of using an OCR technique for determining if the actual character marking on the semiconductor is defective. It is believed that Iwakiri et al in combination with Shyu et al meet the added limitation. Although Iwakiri et al's teachings may be intended for determining how to better inscribe

the semiconductor, the method of determining this categorizes the character marking as good or defective.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Allyson N. Trail* whose telephone number is (571) 272-2406. The examiner can normally be reached between the hours of 7:30AM to 4:00PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee, can be reached on (571) 272-2398. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**allyson.trail@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Allyson N. Trail
Patent Examiner
Art Unit 2876
May 1, 2005

Jared J. Fureman

JARED J. FUREMAN
PRIMARY EXAMINER